In the claims:

All claims in the application are indicated below.

Claims 1-39 (Canceled)

40. (Previously presented) A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a first surface, a transistor located within the semiconductor substrate for amplifying charges, a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin located a first distance from the transistor, a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin located a second distance from the transistor, and a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor overlapping a portion of the depletion prevention region margin and the charge accumulation region margin, the charge accumulation region margin being closer to the transistor than the depletion prevention margin, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor, the substrate and the depletion prevention region have different impurity concentrations, the method comprising the steps:

implanting ions of the first conductive type at a first angle to the first surface of the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and doesn't contact the first surface of the semiconductor substrate; and

implanting ions of the second conductive type at a second angle to the first surface of the semiconductor substrate using the transfer gate as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the first surface of the semiconductor substrate;

wherein the first angle is not greater than the second angle, thereby causing the first distance of the charge accumulation region margin to the transistor to be no greater than the second distance of depletion prevention region margin to the transistor.

41. (Previously presented) The method of claim 40 wherein the first angle is between 30 degrees and 80 degrees and the second angle is substantially 90 degrees.

42. (Previously presented) The method of claim 40 wherein the first angle is between 40 degrees and 60 degrees and the second angle is substantially 90 degrees.

43. (Previously presented) The method of claim 40 wherein the first angle is between 30 degrees and 80 degrees and the second angle is between 80 degrees and 90 degrees.

44. (Previously presented) The method of claim 40 wherein the first angle and the second angle are substantially equal and the charge accumulation region margin and the depletion prevention region margin are substantially the same distance from the transistor.

45. (Previously presented) The method of claim 40 wherein the second distance of the depletion region margin to the transistor is between 0.0 μm and 0.2 μm greater than the first distance of the charge accumulation region margin to the transistor.

46. (Previously presented) The method of claim 40 wherein the depth of the charge accumulation region from the first surface is between 0.6 μm and 0.8 μm and the maximum impurity concentrations of the charge accumulation region is between 1×10^{17} and 2×10^{17} per cm^3, and the first angle is between 66 degrees and 75 degrees and the second angle is between 80 degrees and 90 degrees.

Claims 47-55 (Cancelled)